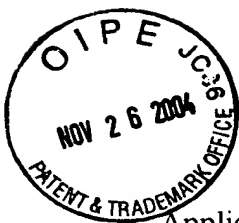


**Amendments to the Drawings**

The attached Replacement Sheets of drawings includes changes to **Figures 4, 12, 13, 14, 15, and 32** addressing the Examiner's objections. In each of the figures, previously omitted descriptive wording has been added. No new matter has been added. In addition to the replacement sheets, formal replacement sheets are supplied for all other sheets.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Epps, Garry P.; Laor, Michael  
Assignee: Cisco Technology, Inc.  
Title: Pipelined Packet Switching And Queuing Architecture  
Serial No.: 09/503,552 Filing Date: February 14, 2000  
Examiner: Kevin C. Harper Group Art Unit: 2666  
Docket No.: CIS0021US Client Ref. No.: 1506

RECEIVED Austin, Texas  
November 22, 2004

DEC 02 2004  
Technology Center 2600

Mail Stop Amendment  
Attention: Official Draftsperson  
COMMISSIONER FOR PATENTS  
P. O. Box 1450  
Alexandria, VA 22313-1450

**SUBMISSION OF FORMAL DRAWINGS**

Dear Sir:

Applicants submit twenty-seven (27) sheets of formal drawings, consisting of Figures 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16 & 19, 17, 18, 20 & 21, 22 & 23, 24 & 25, 26, 27, 28, 29, 30 & 31, and 32; in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (512) 439-5085.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Attention: Mail Stop Amendment, Attn: Official Draftsperson, Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on November 22, 2004.

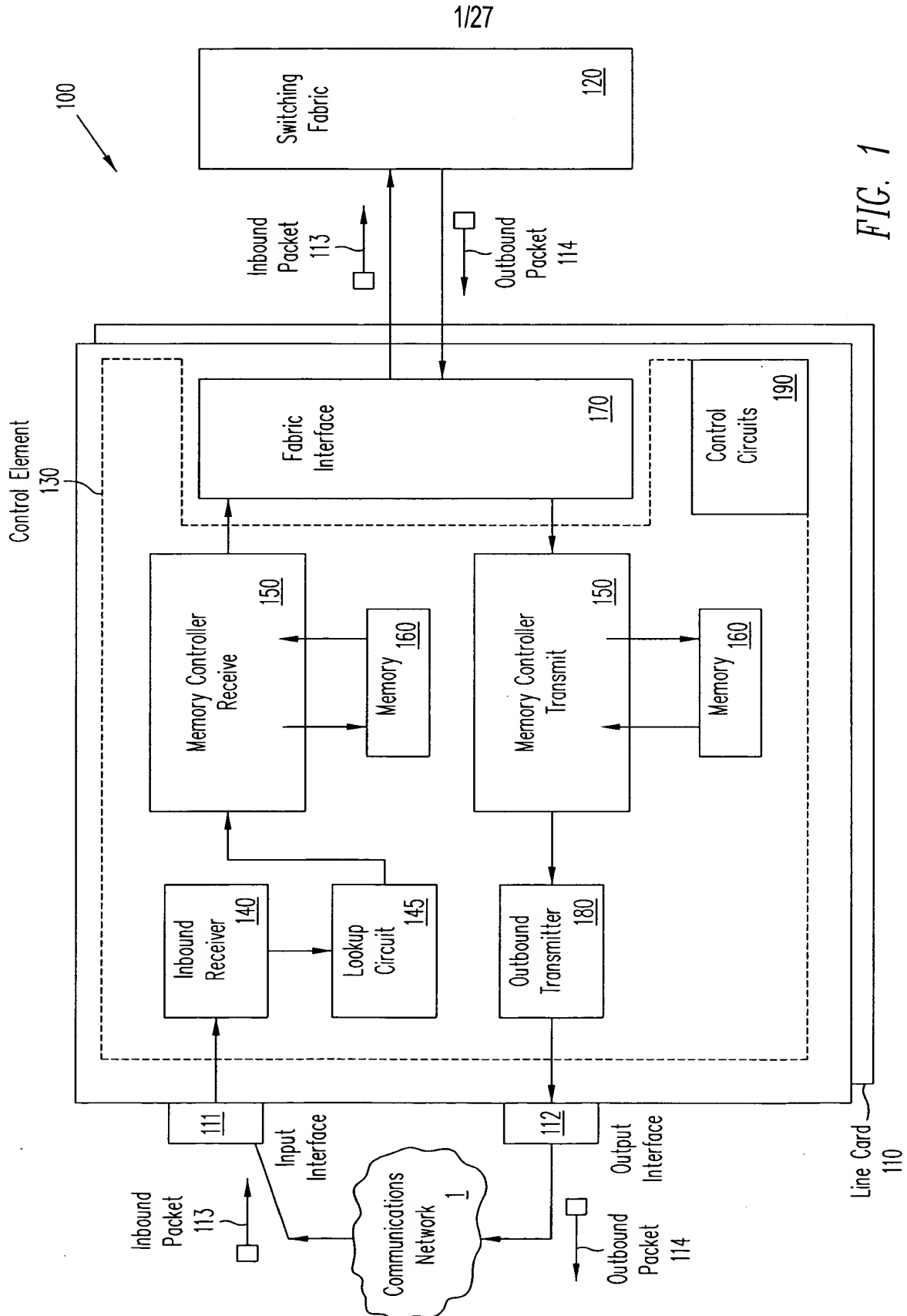
  
Attorney for Applicant(s)

11/22/04  
Date of Signature

Respectfully submitted,



Marc R. Ascolese  
Attorney for Applicants  
Reg. No. 42,268  
(512) 439-5080  
(512) 439-5099 (Facsimile)



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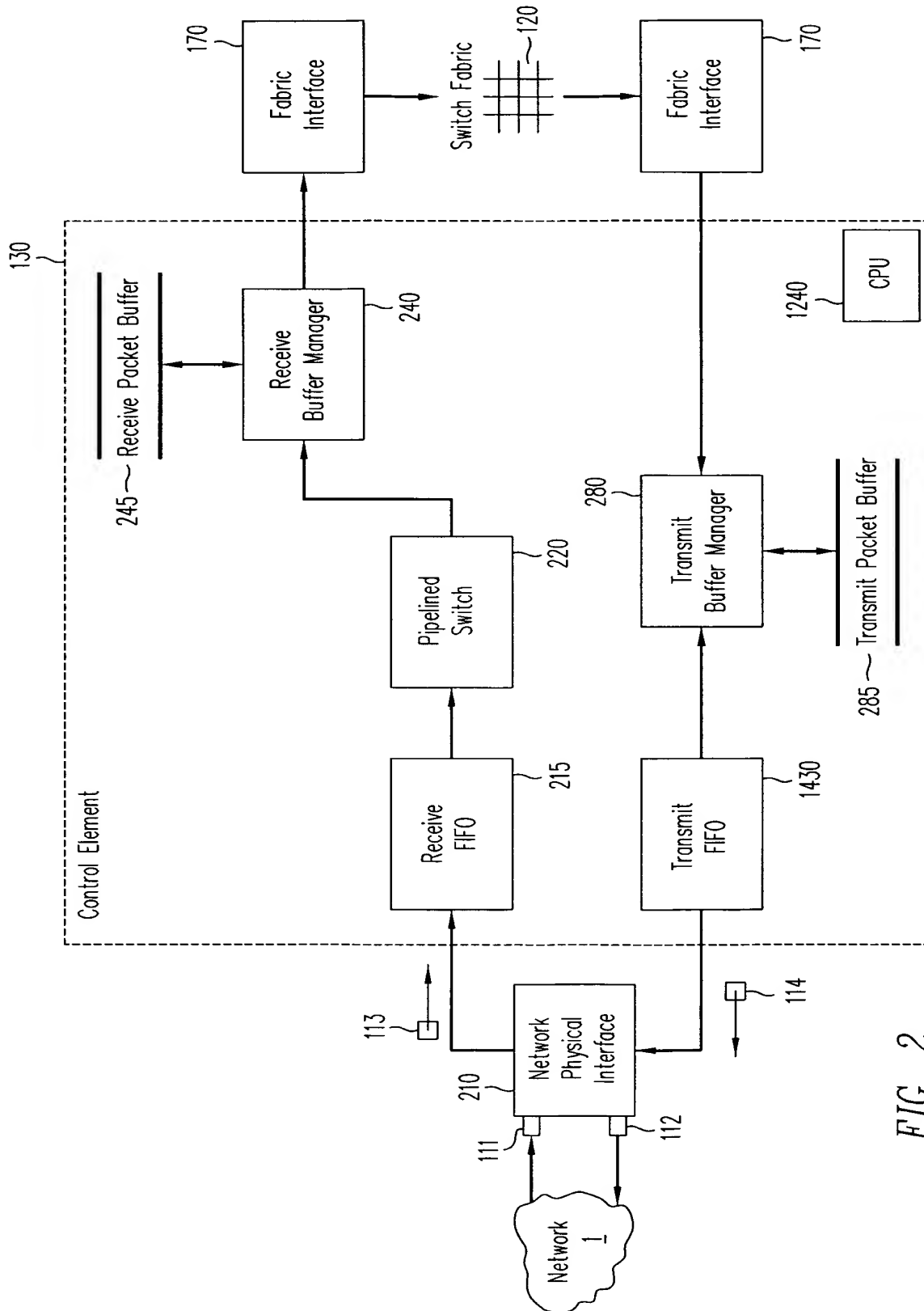


FIG. 2



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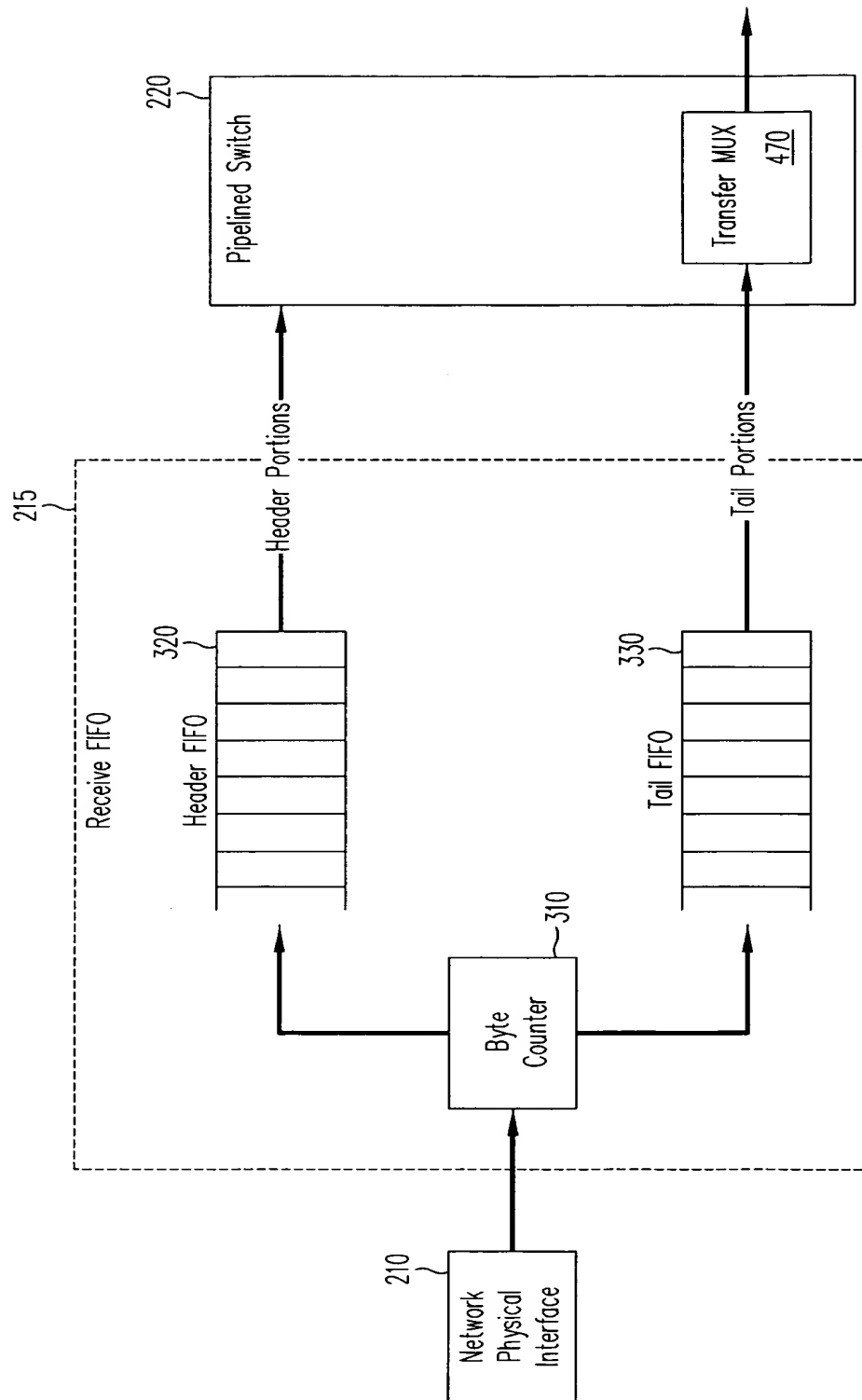


FIG. 3



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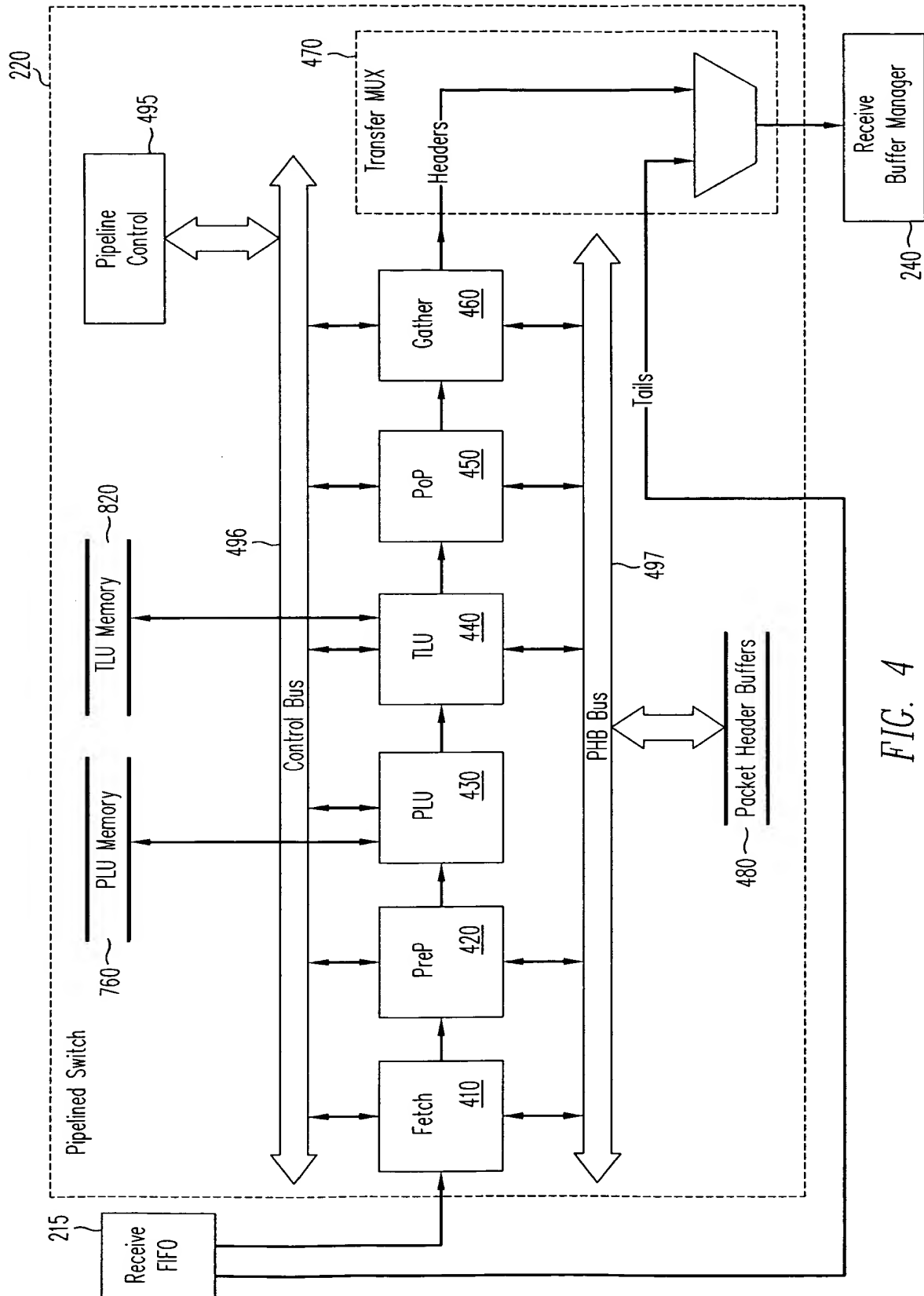


FIG. 4



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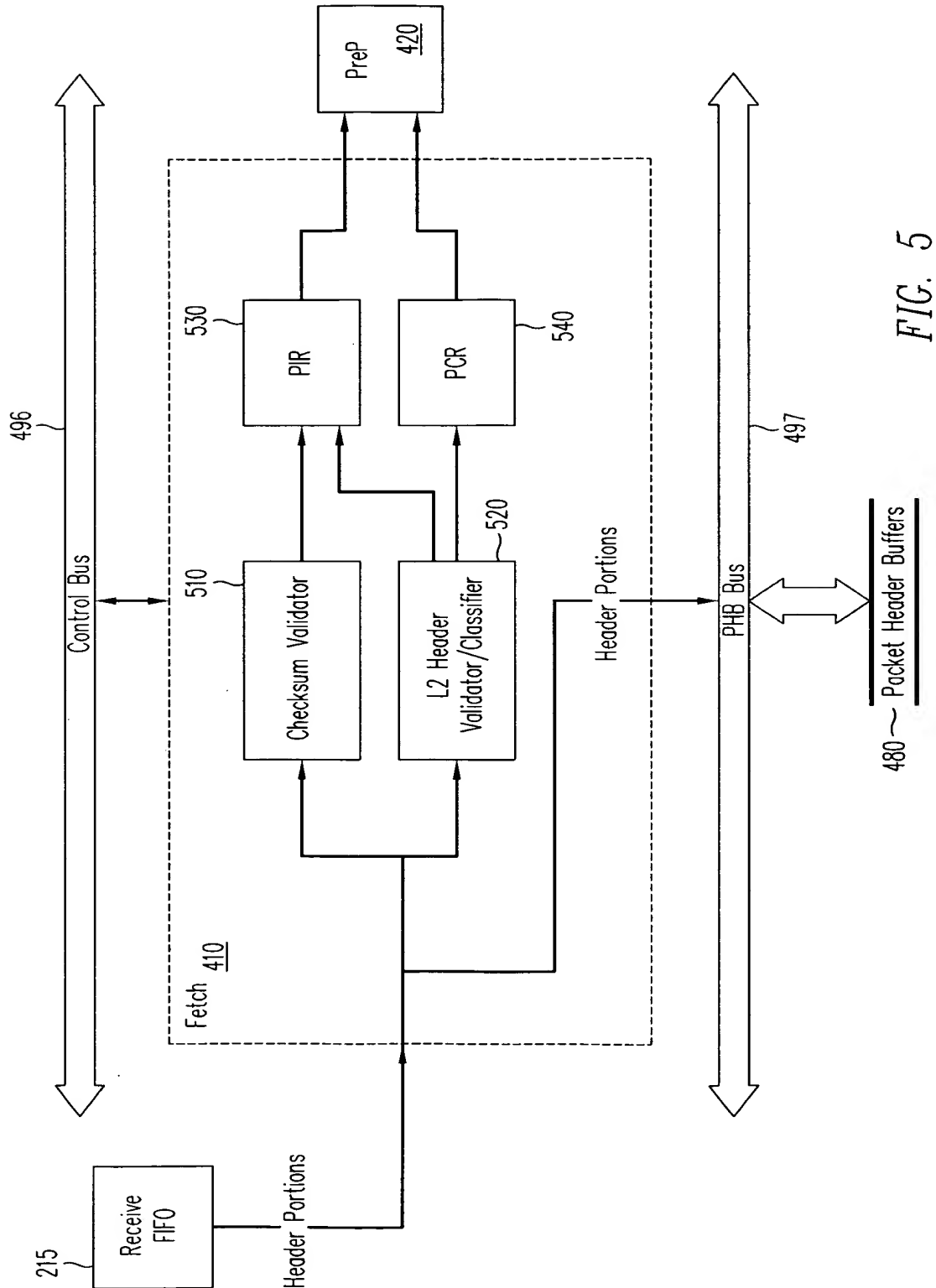
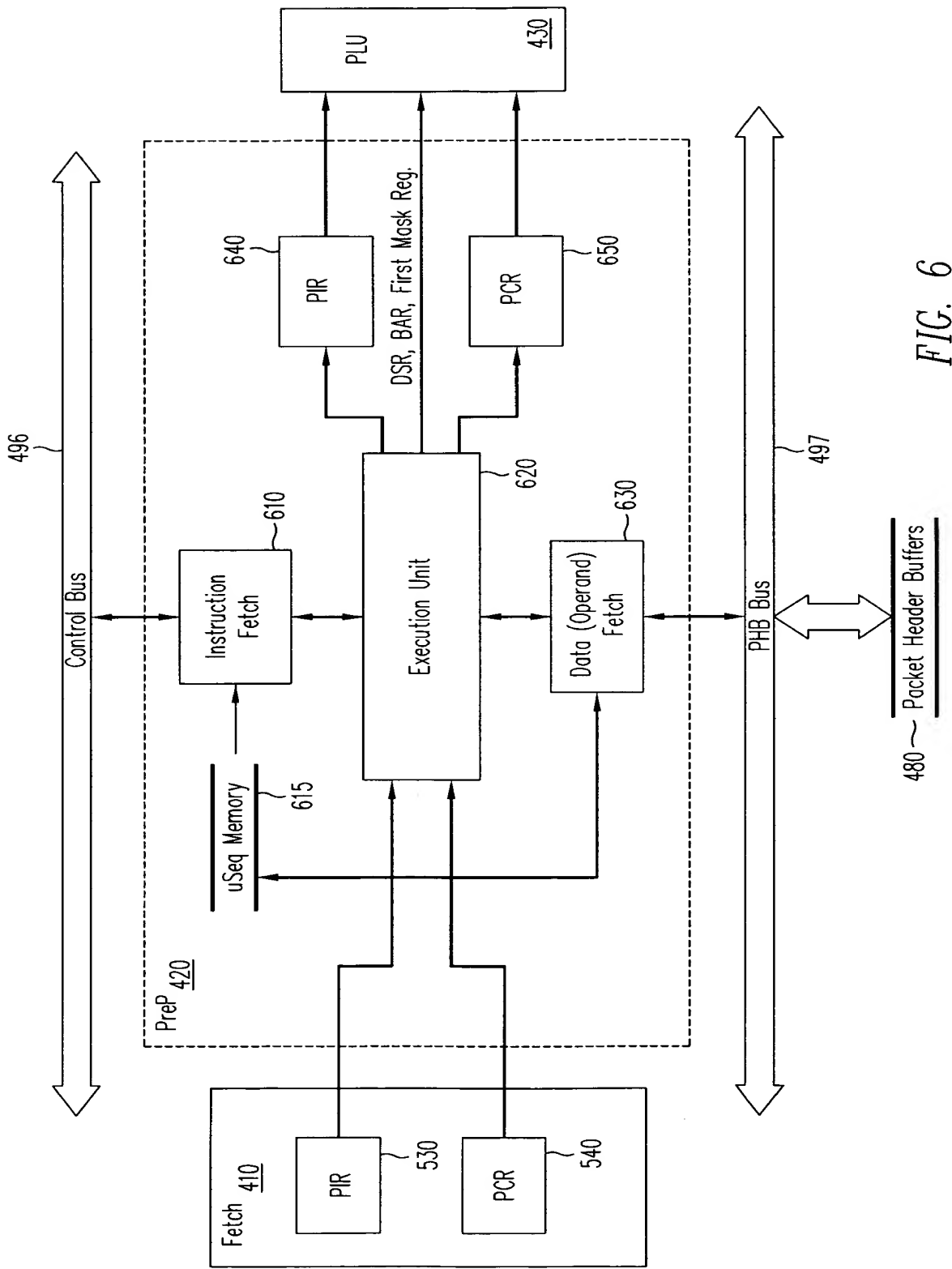


FIG. 5



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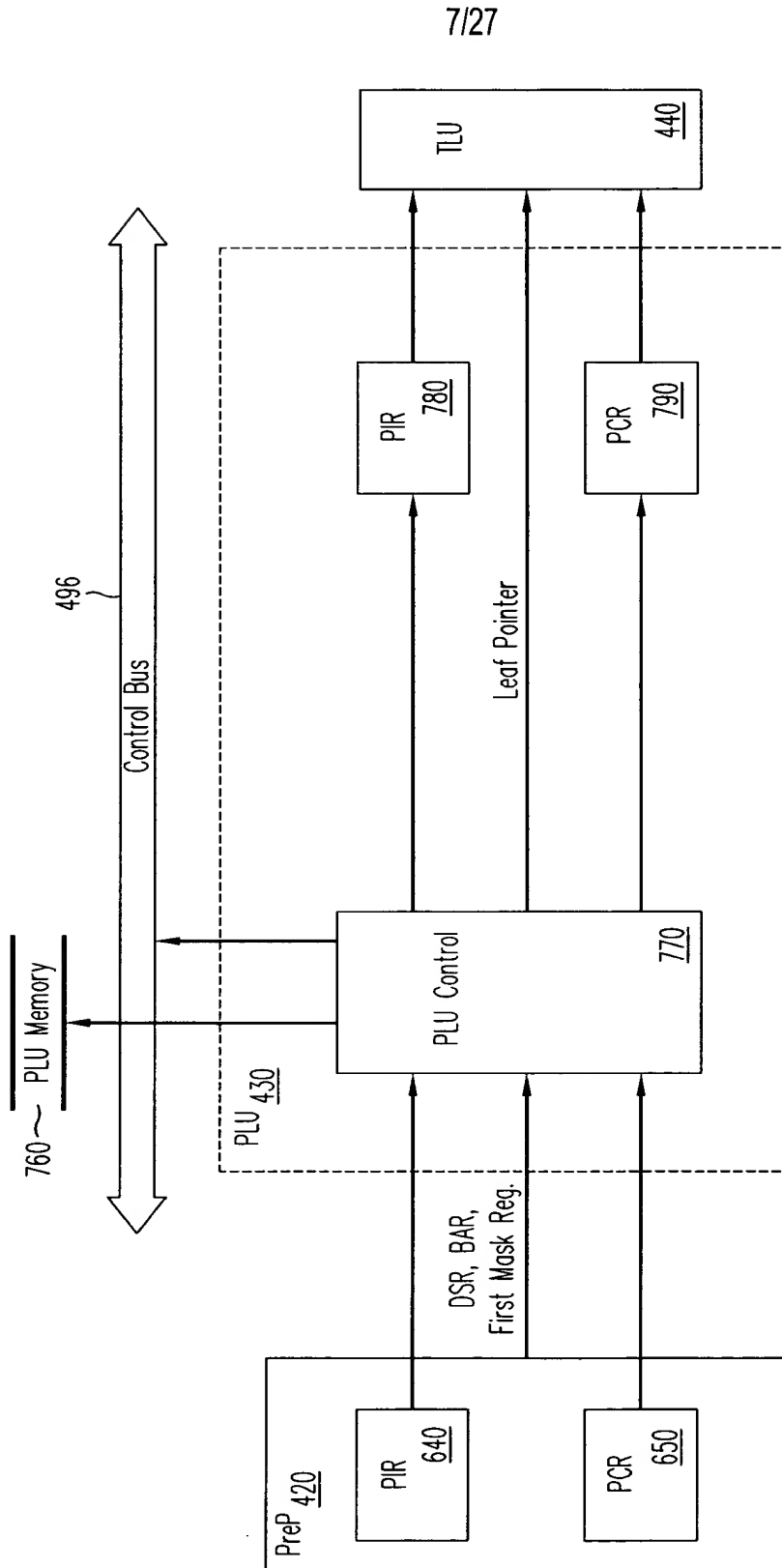
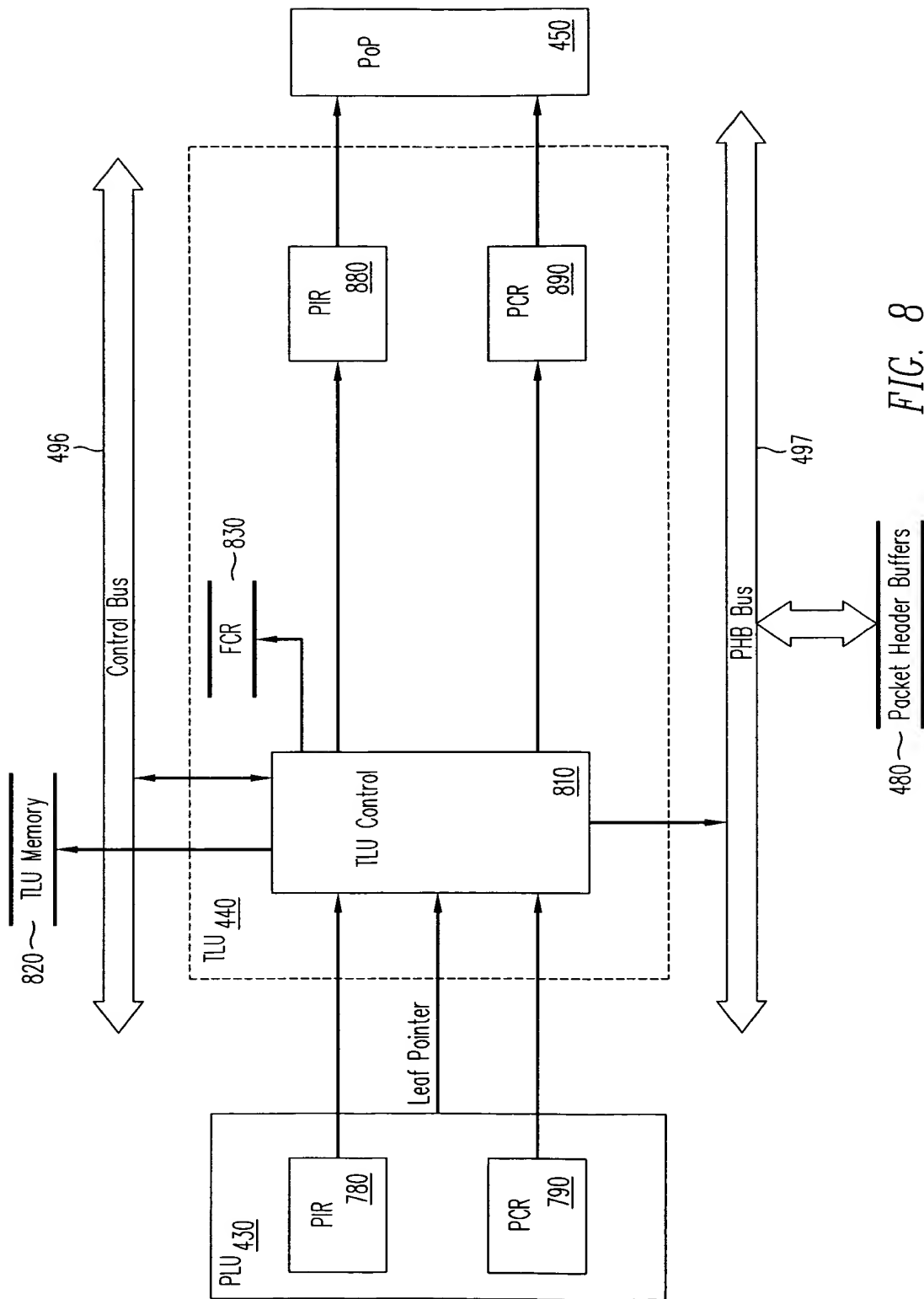


FIG. 7



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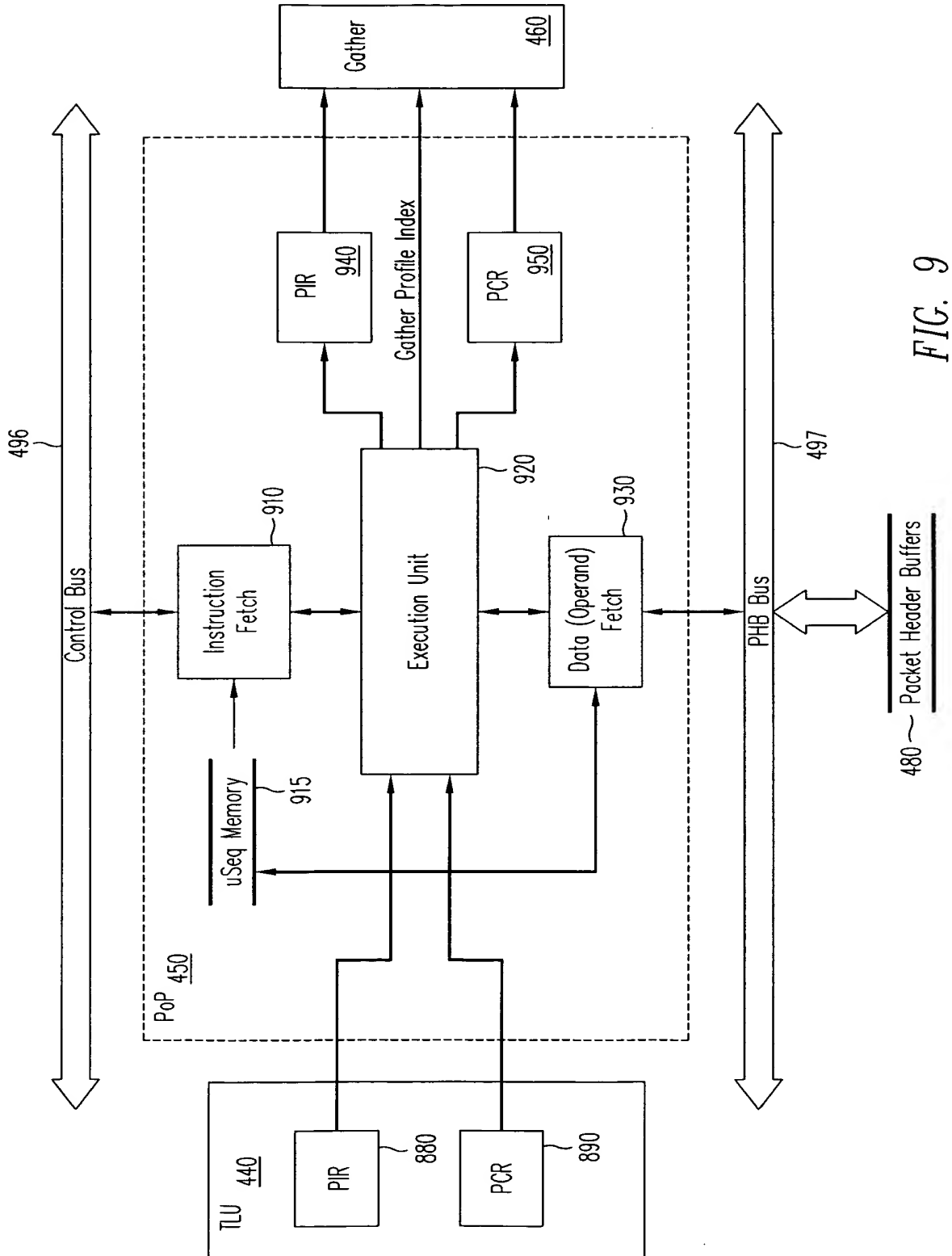


FIG. 9



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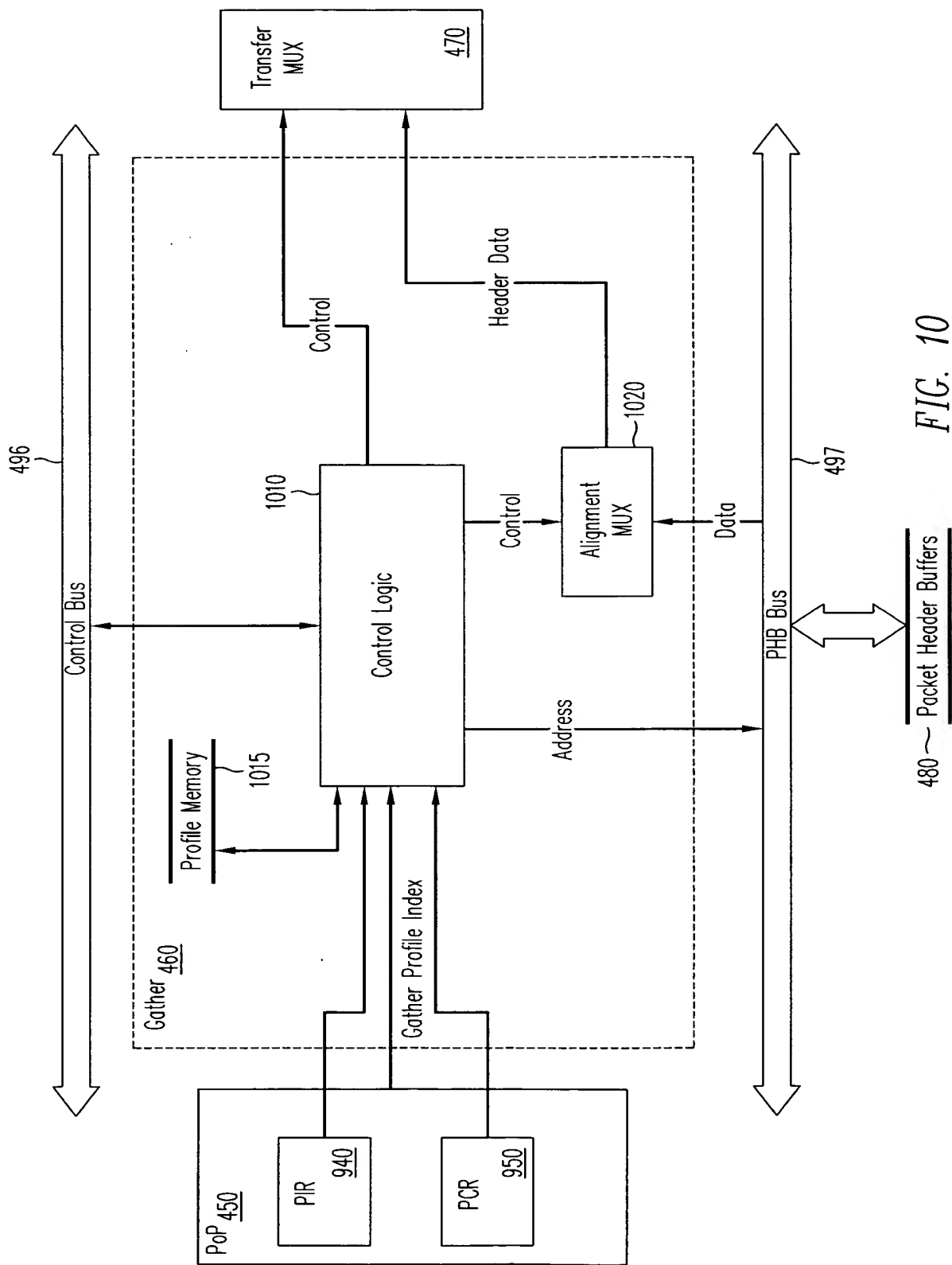


FIG. 10

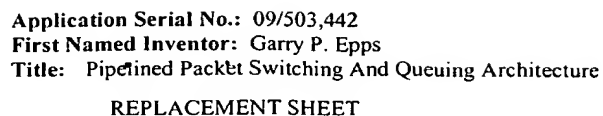


FIG. 11 is a block diagram of a packet transfer system. The system includes a **Receive FIFO** (215) and a **Gather** block (460). The **Receive FIFO** outputs a **Header Portion** to the **Gather** block. The **Gather** block outputs a **Header Portion** to a **MUX Control** block (470) and a **Tail Portion** to a **Transfer MUX** (470). The **MUX Control** block also receives a **Control** signal. The **MUX Control** block outputs **Header Portions** to the **Transfer MUX**. The **Transfer MUX** outputs to an **RBM** (240). The **RBM** outputs **Ready for Heads** and **Ready for Tails** signals back to the **MUX Control** block.

FIG. 11



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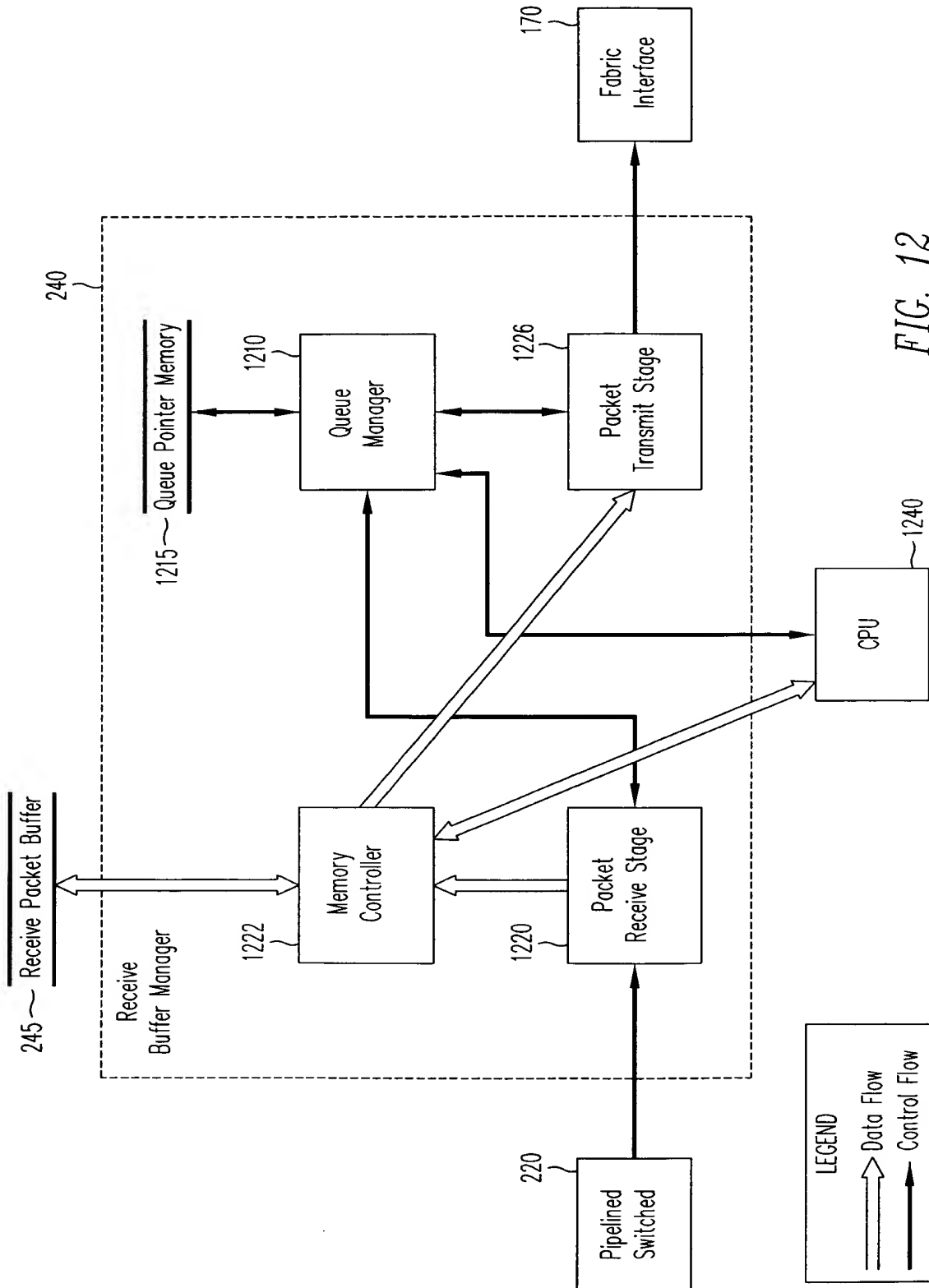


FIG. 12



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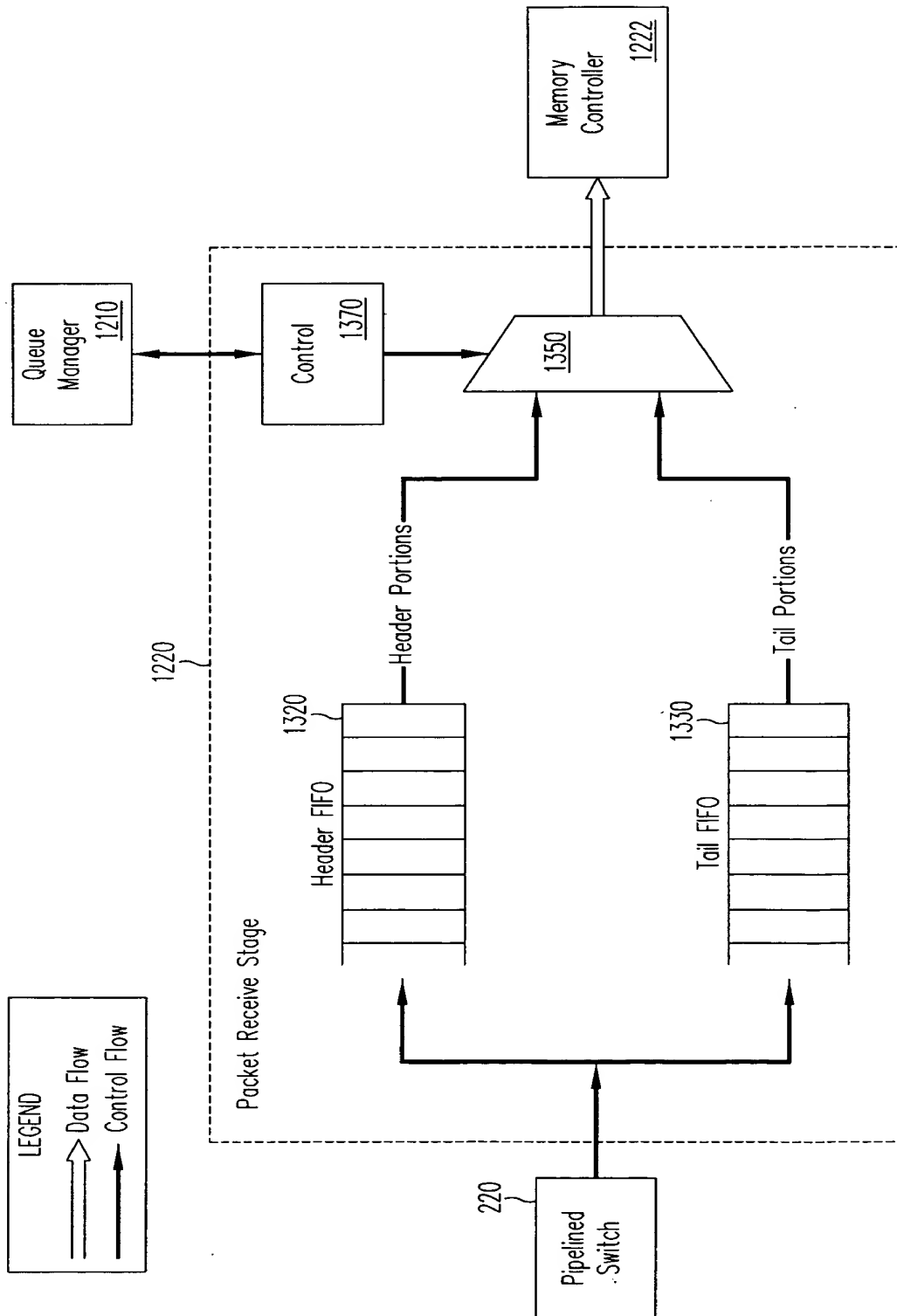


FIG. 13



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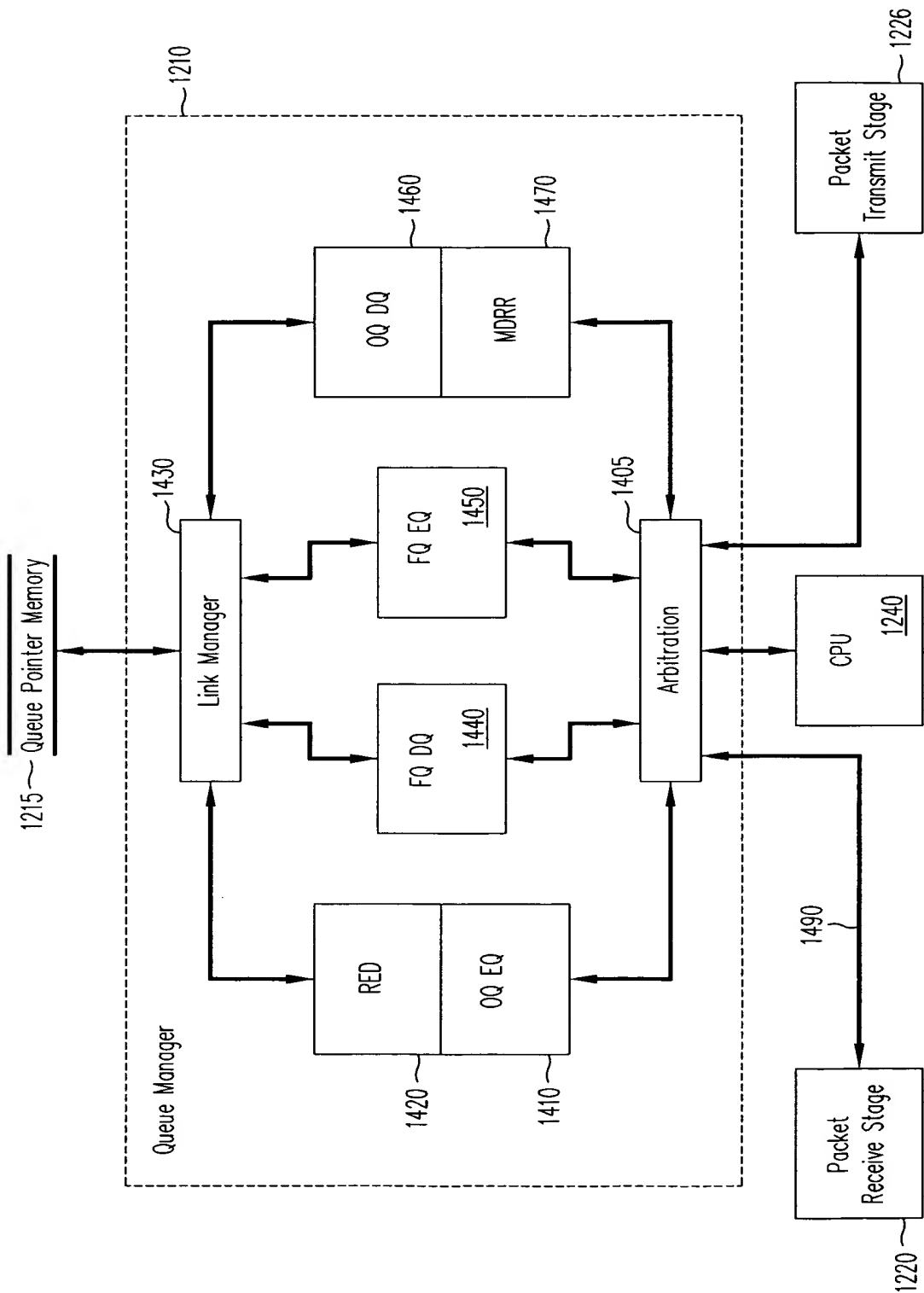
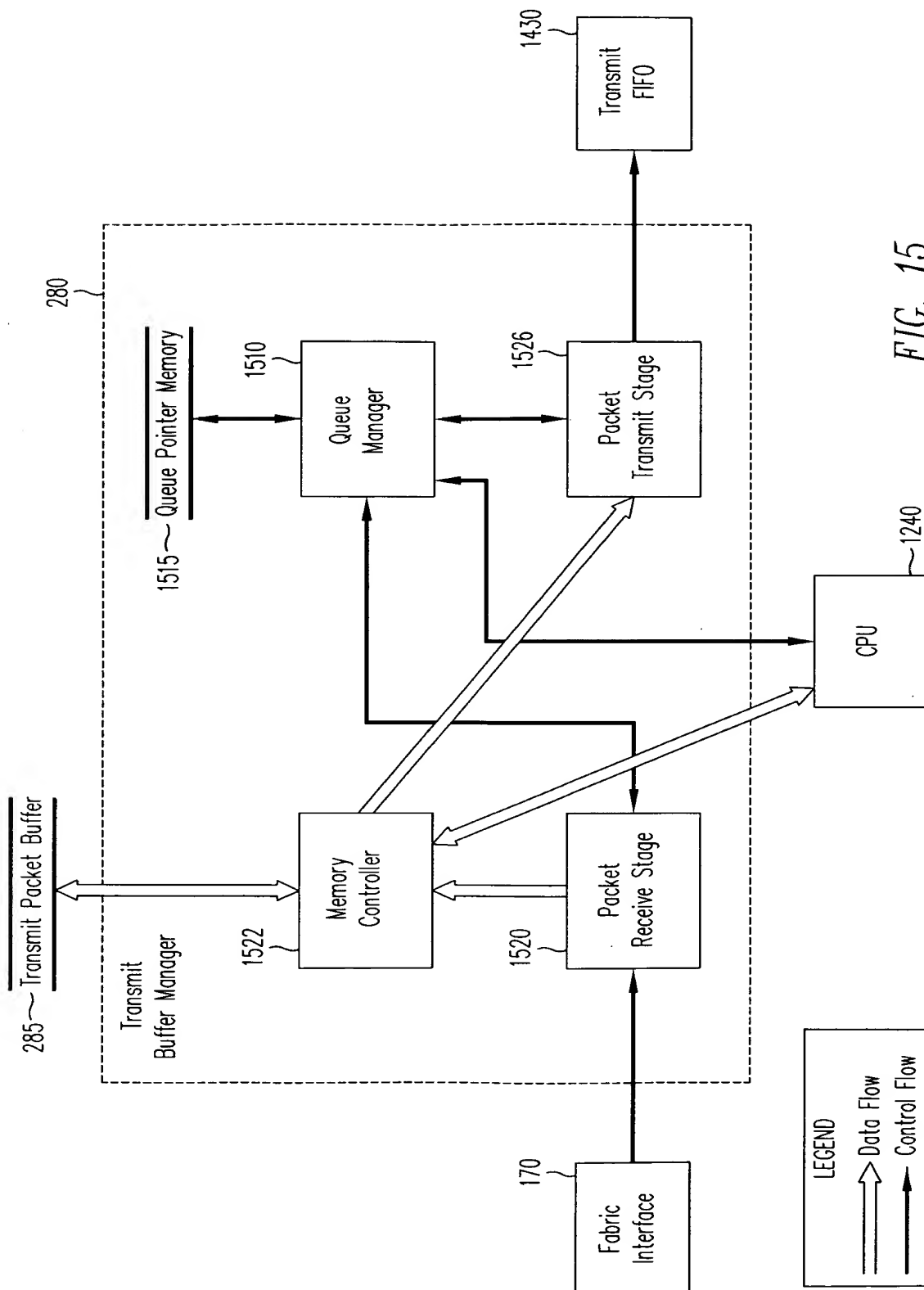


FIG. 14





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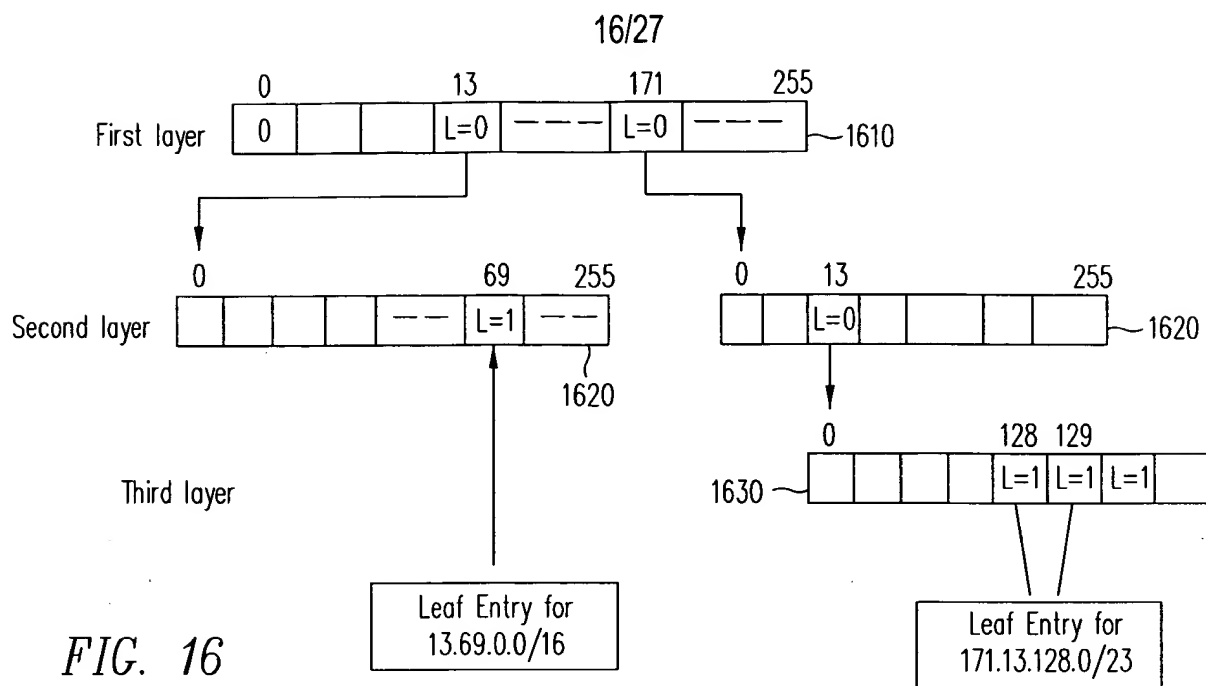


FIG. 16

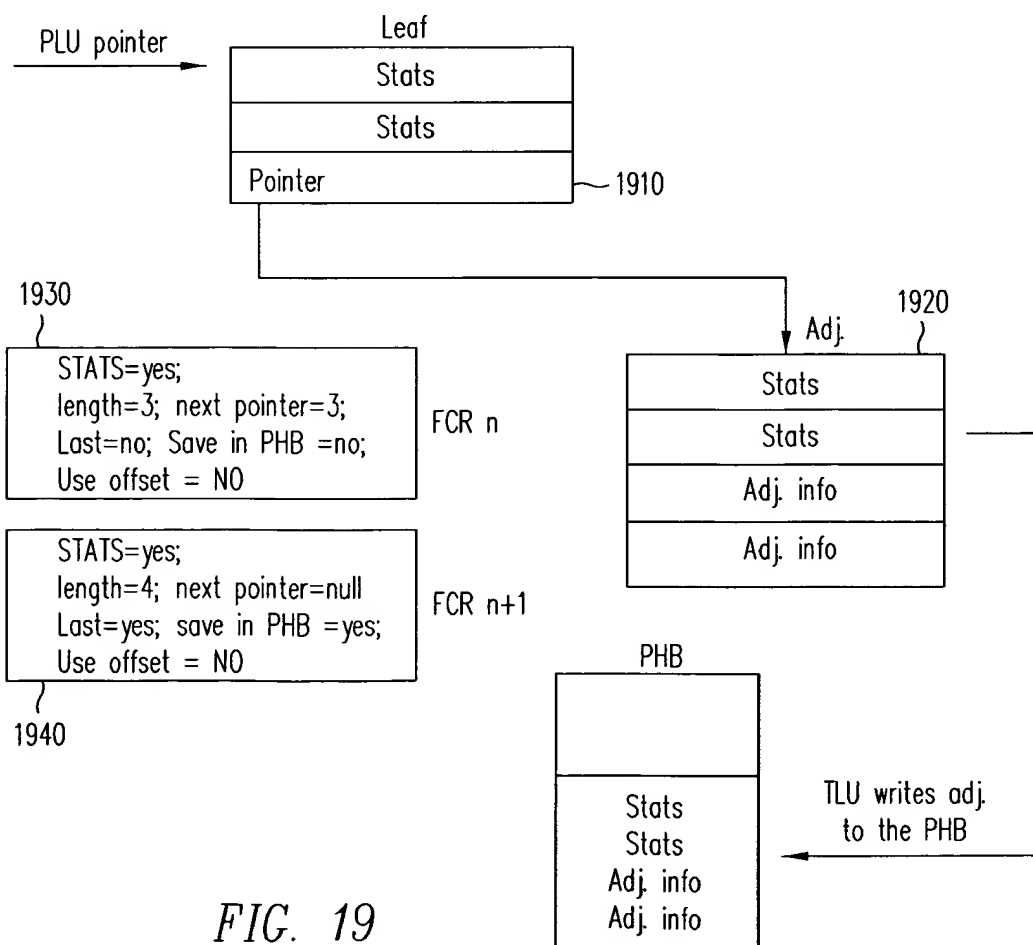
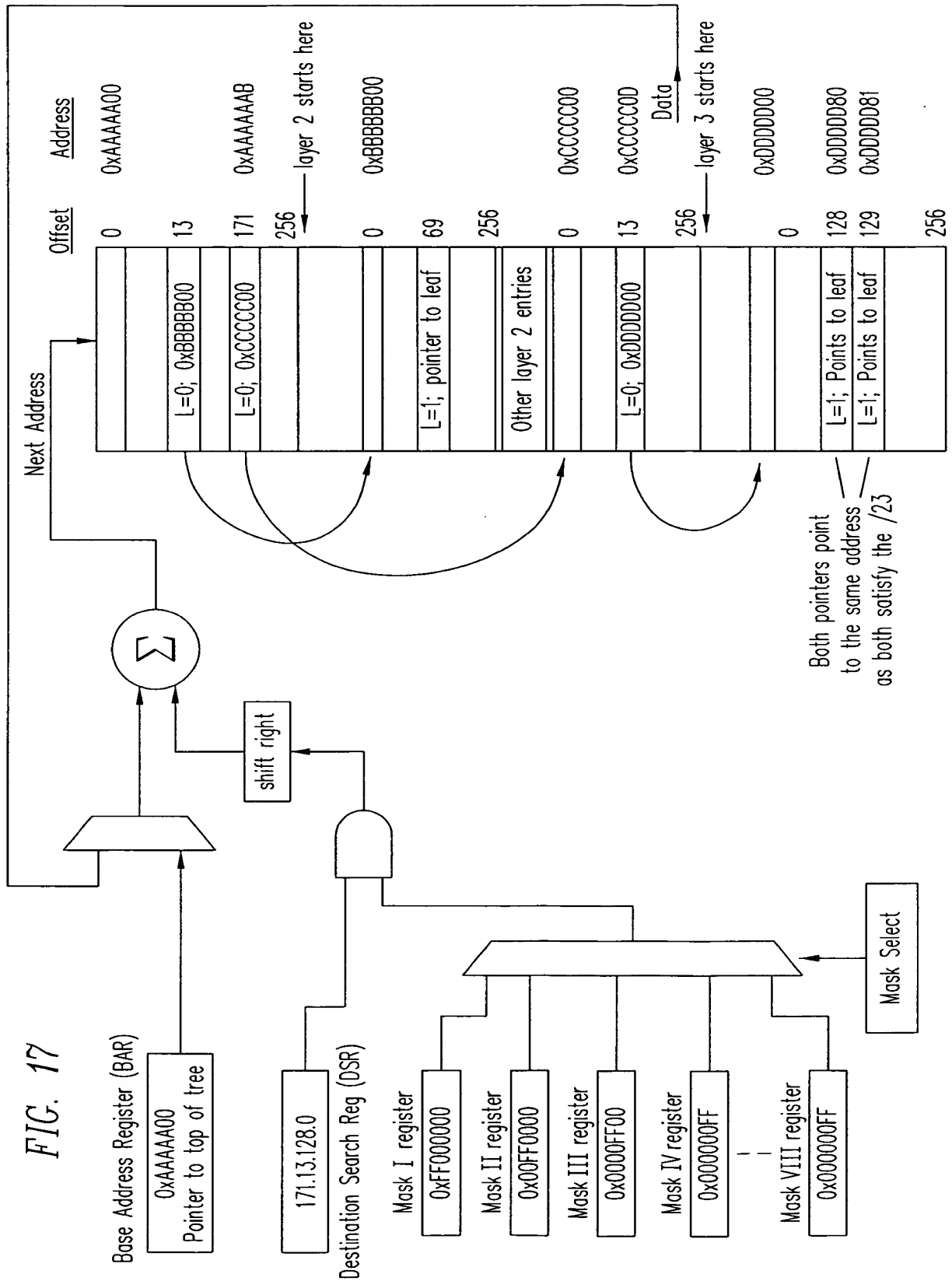


FIG. 19

FIG. 17





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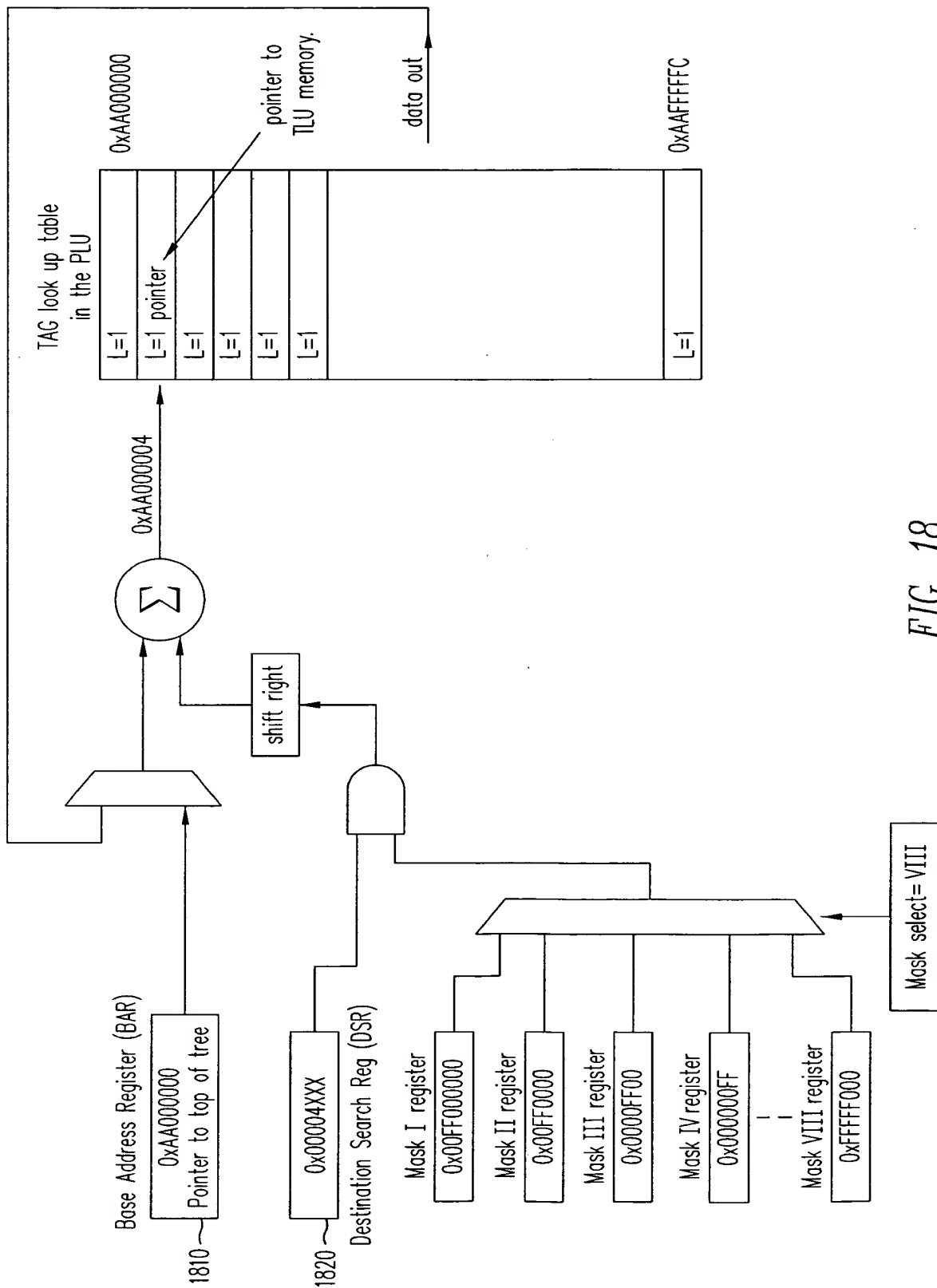
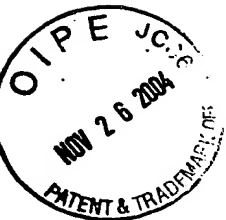
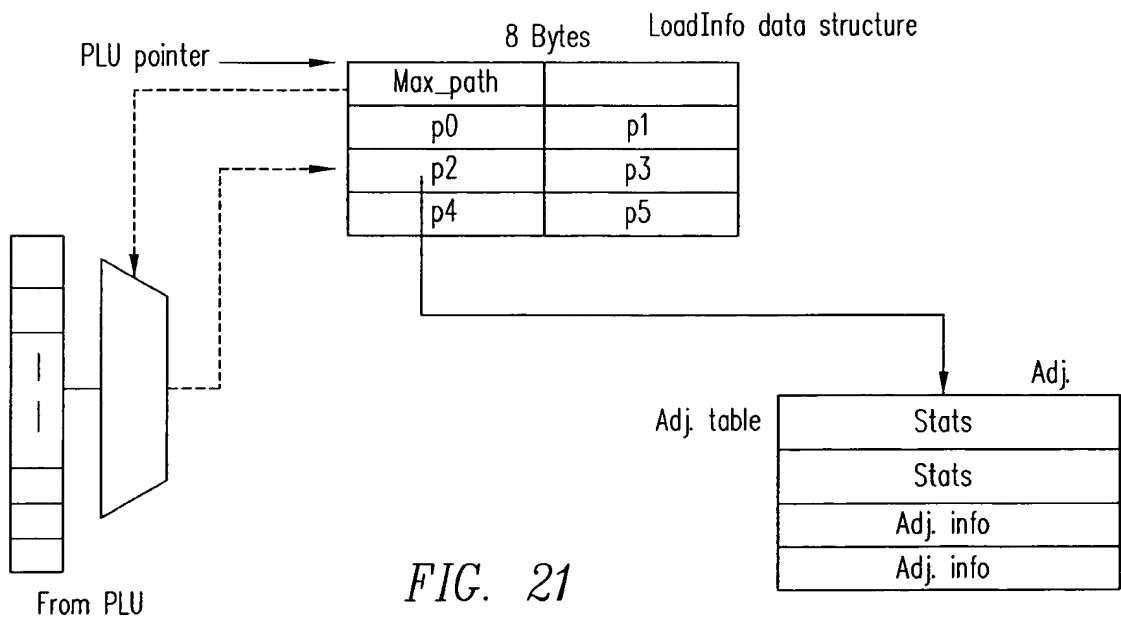
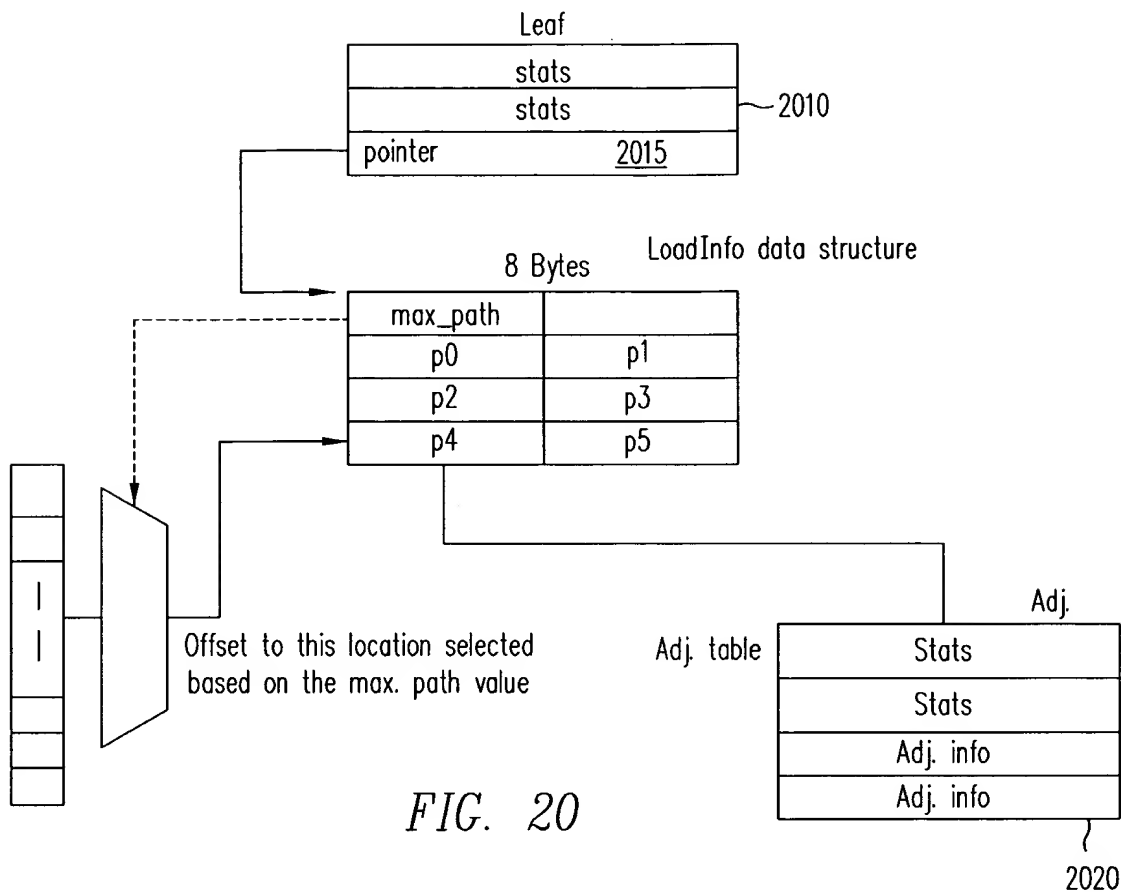


FIG. 18



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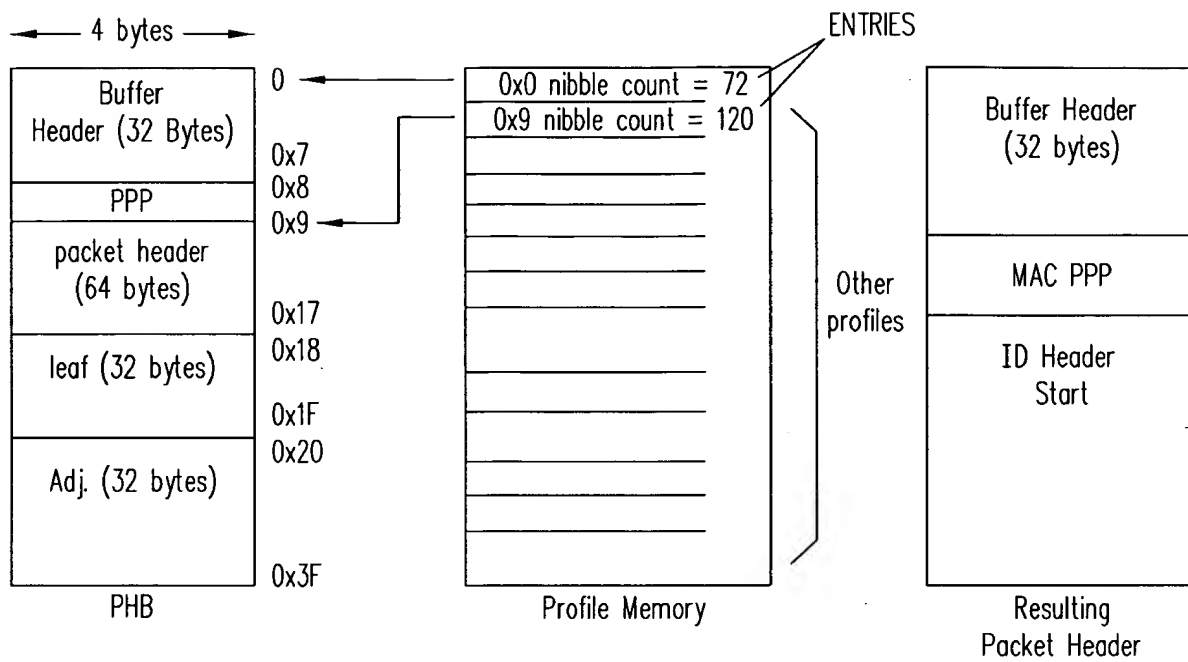


FIG. 22

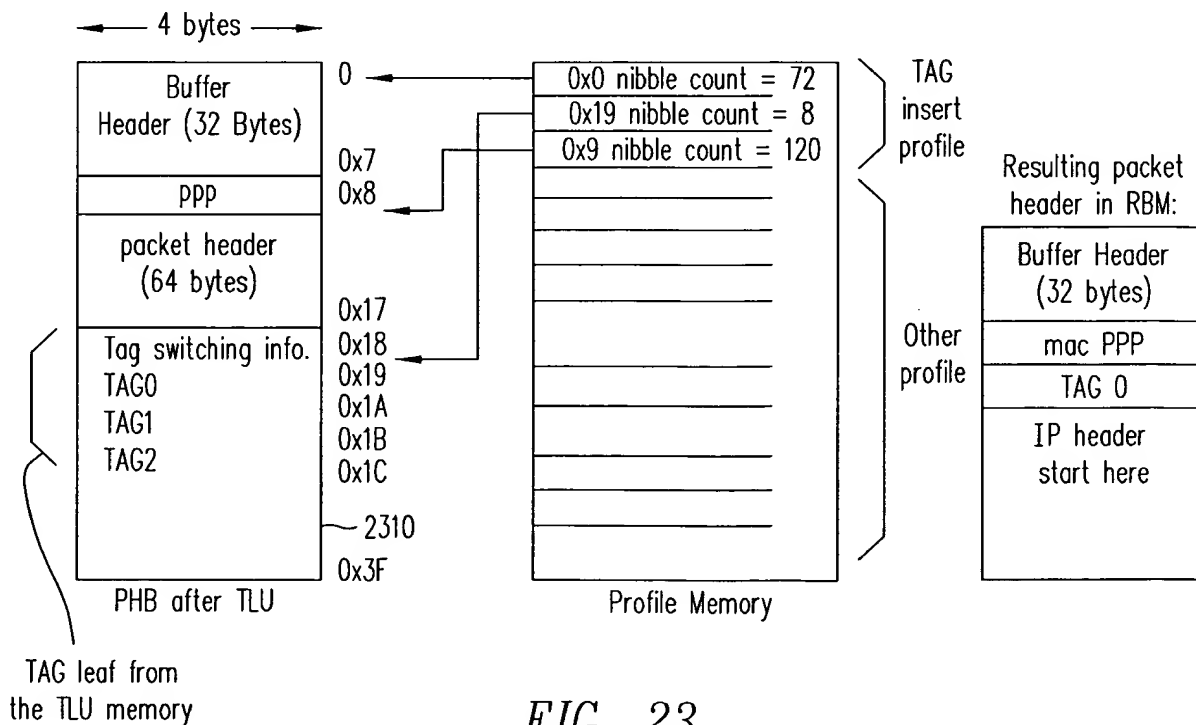


FIG. 23



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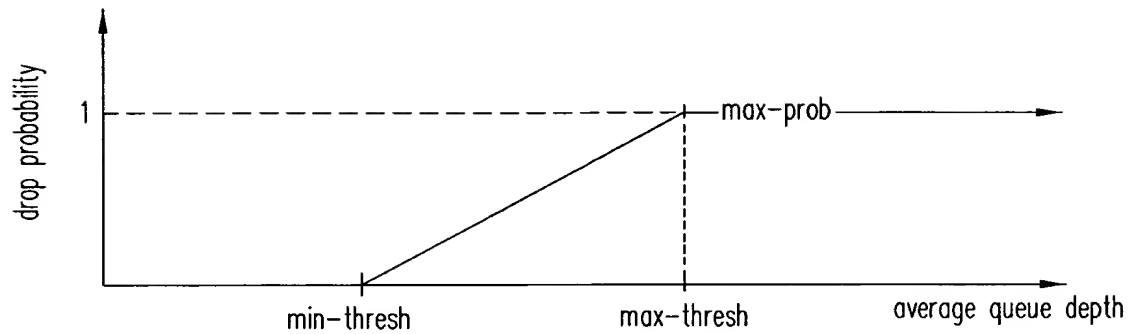


FIG. 24

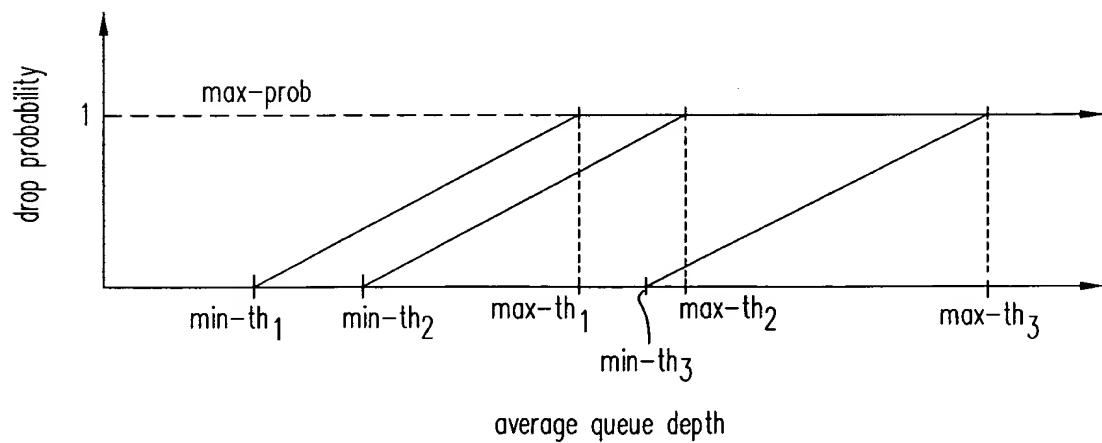
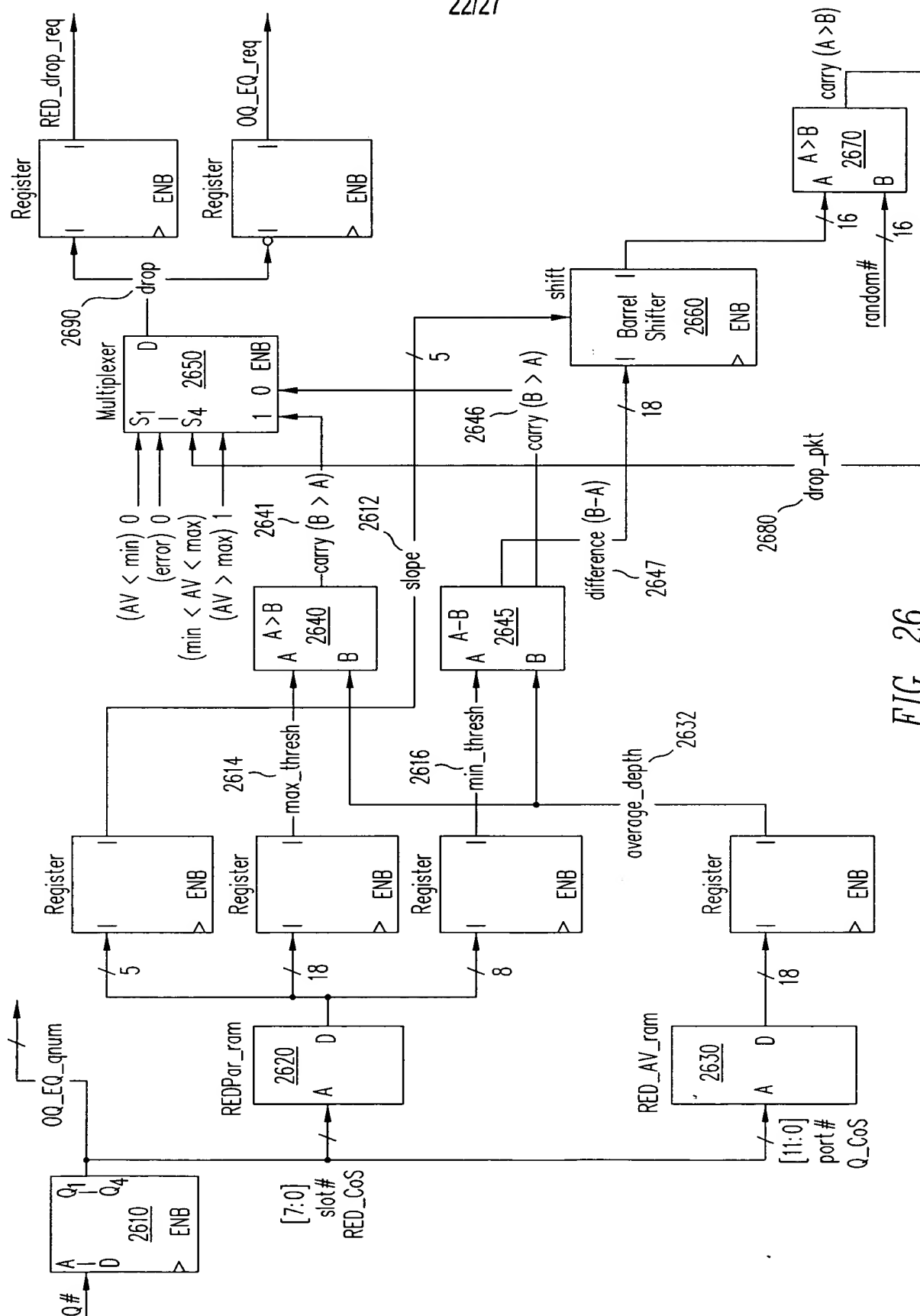
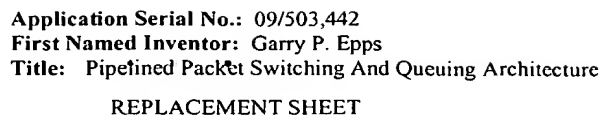


FIG. 25







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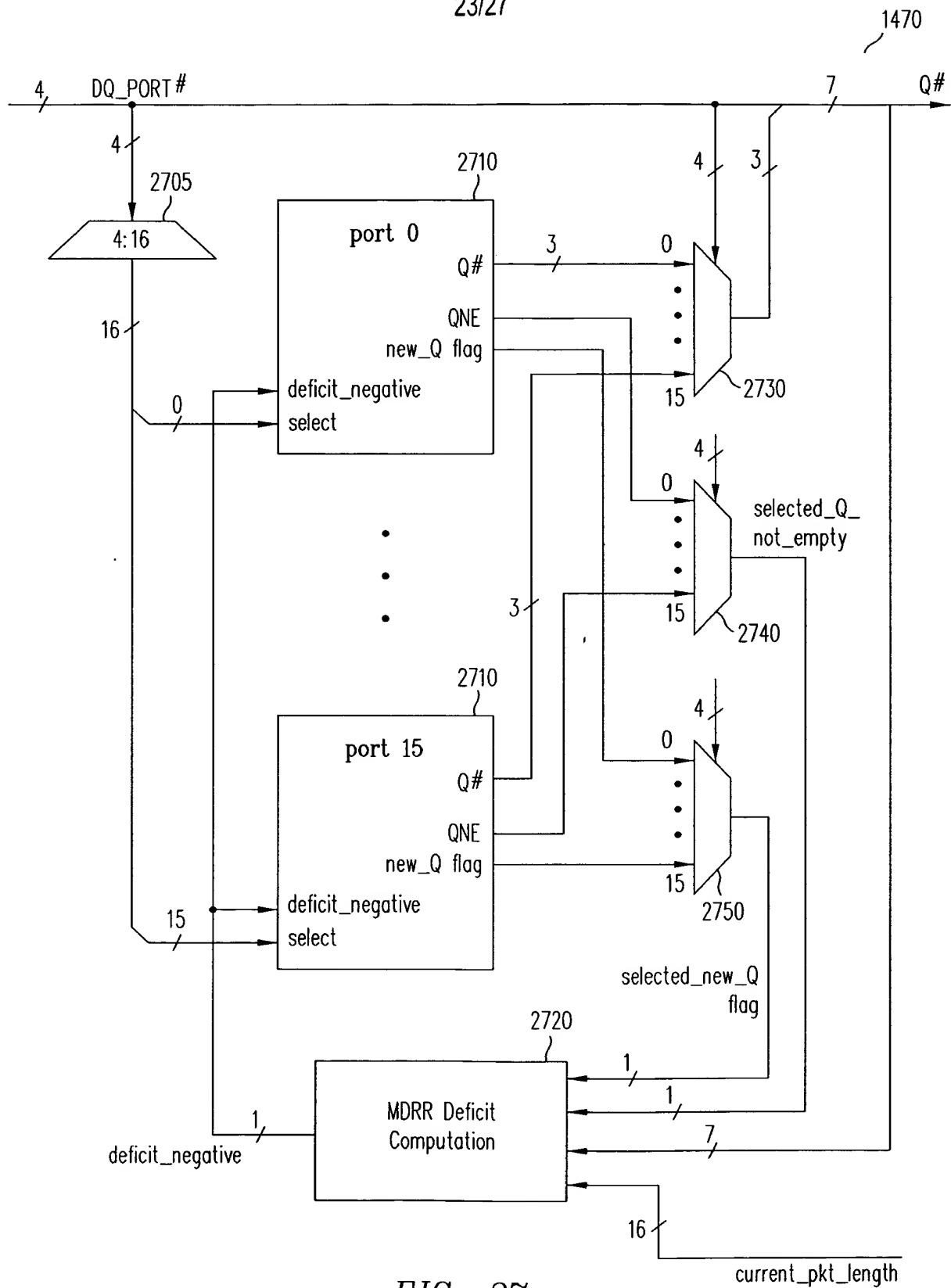
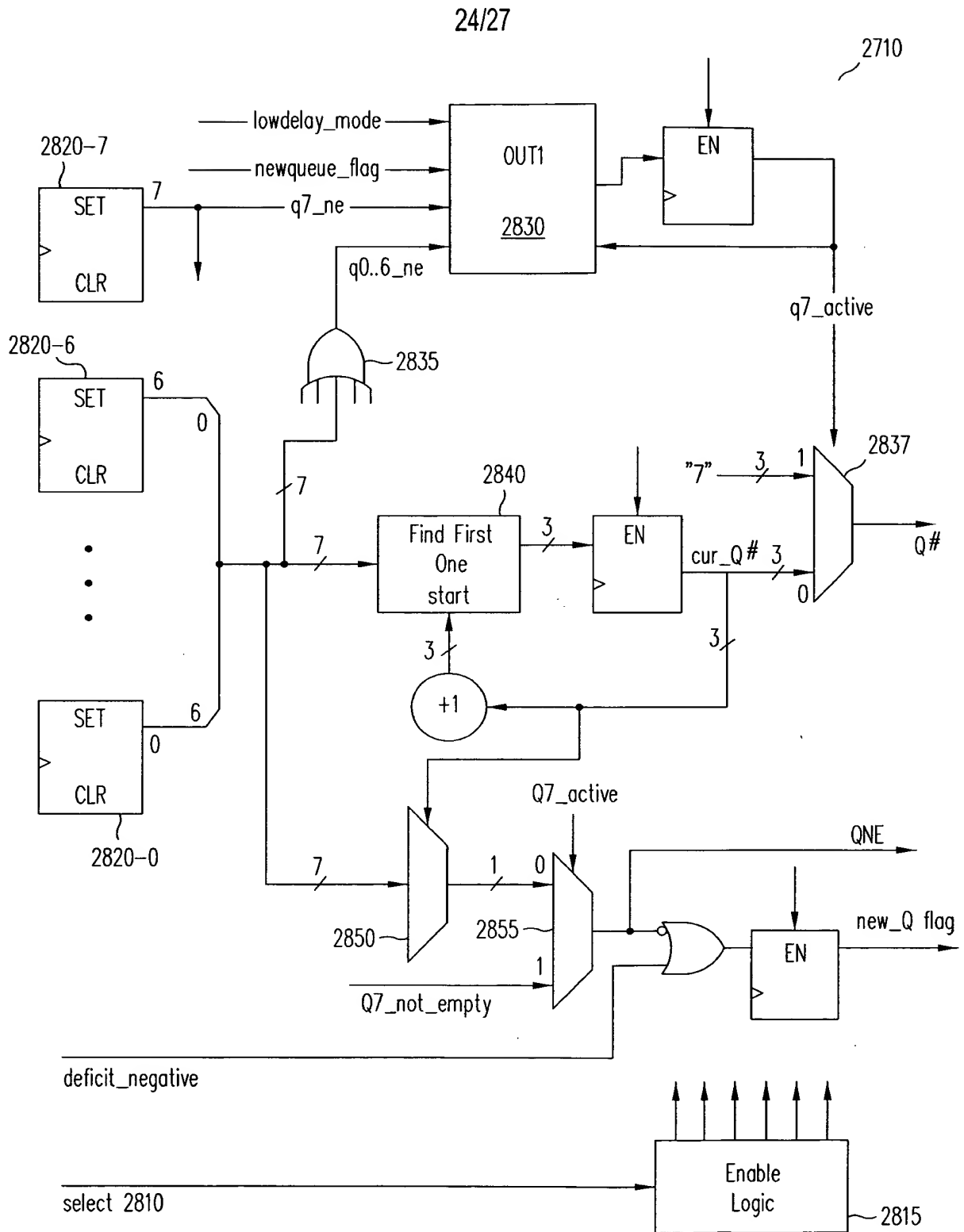
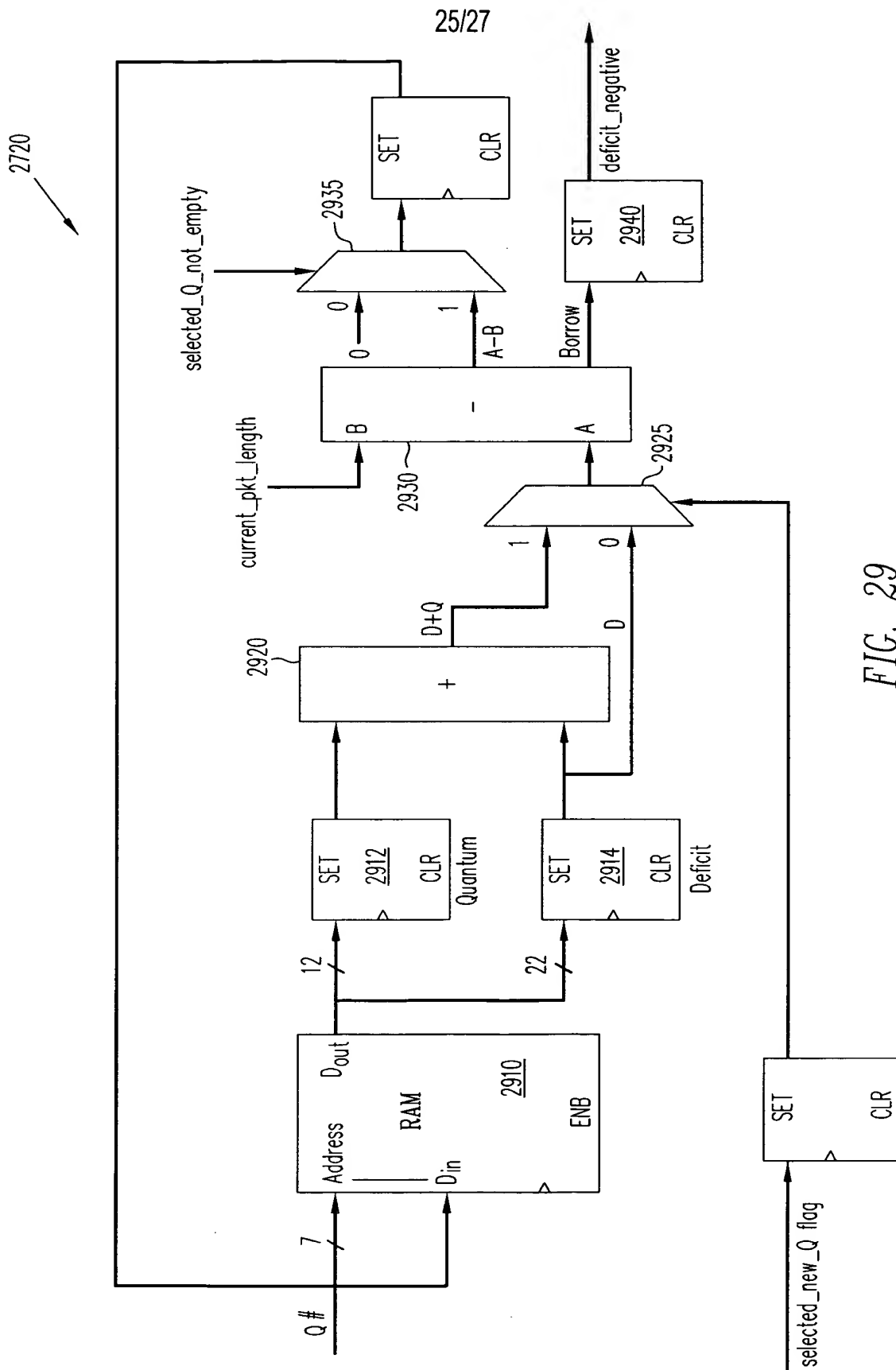


FIG. 27







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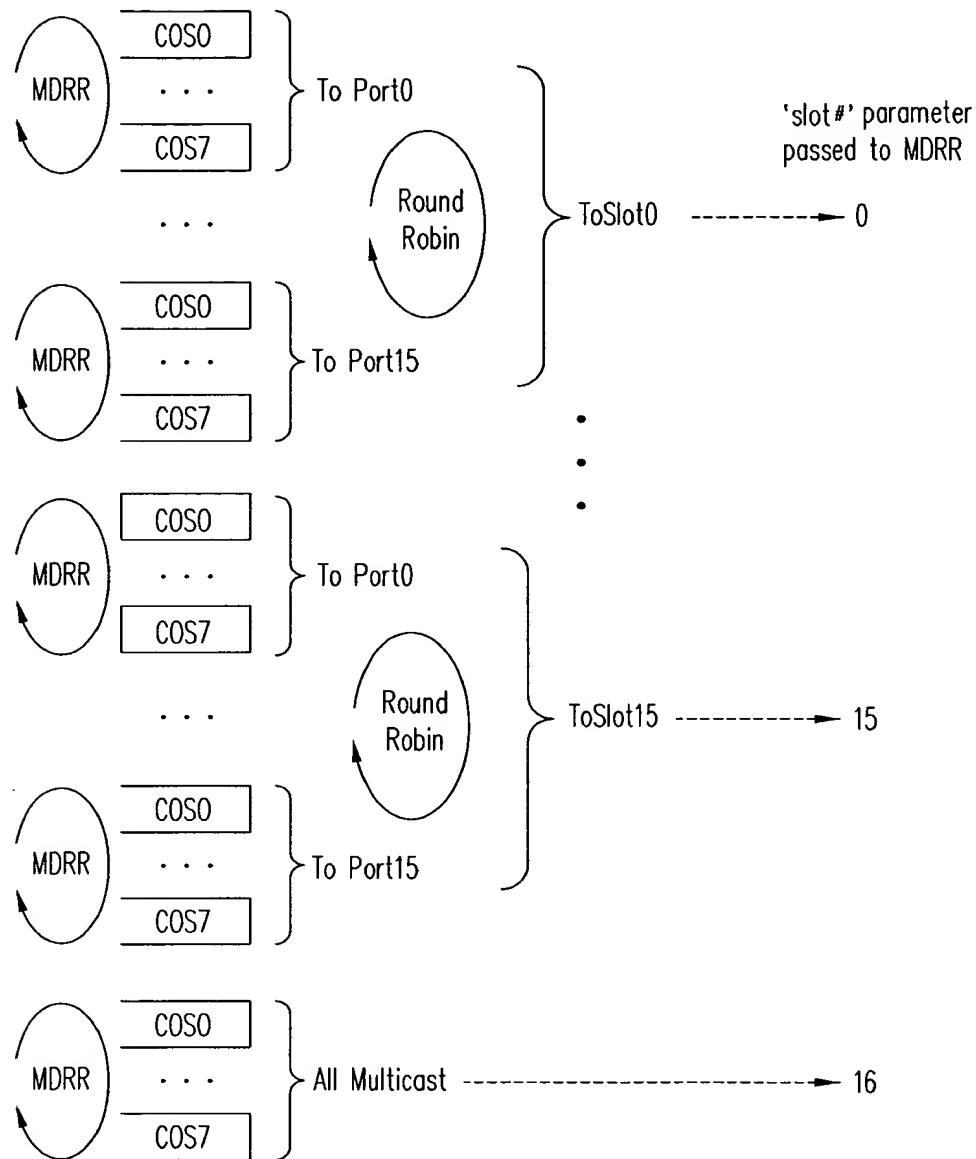


FIG. 30

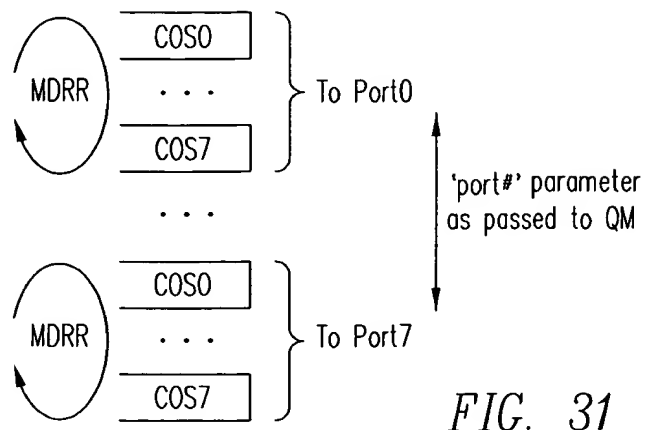


FIG. 31



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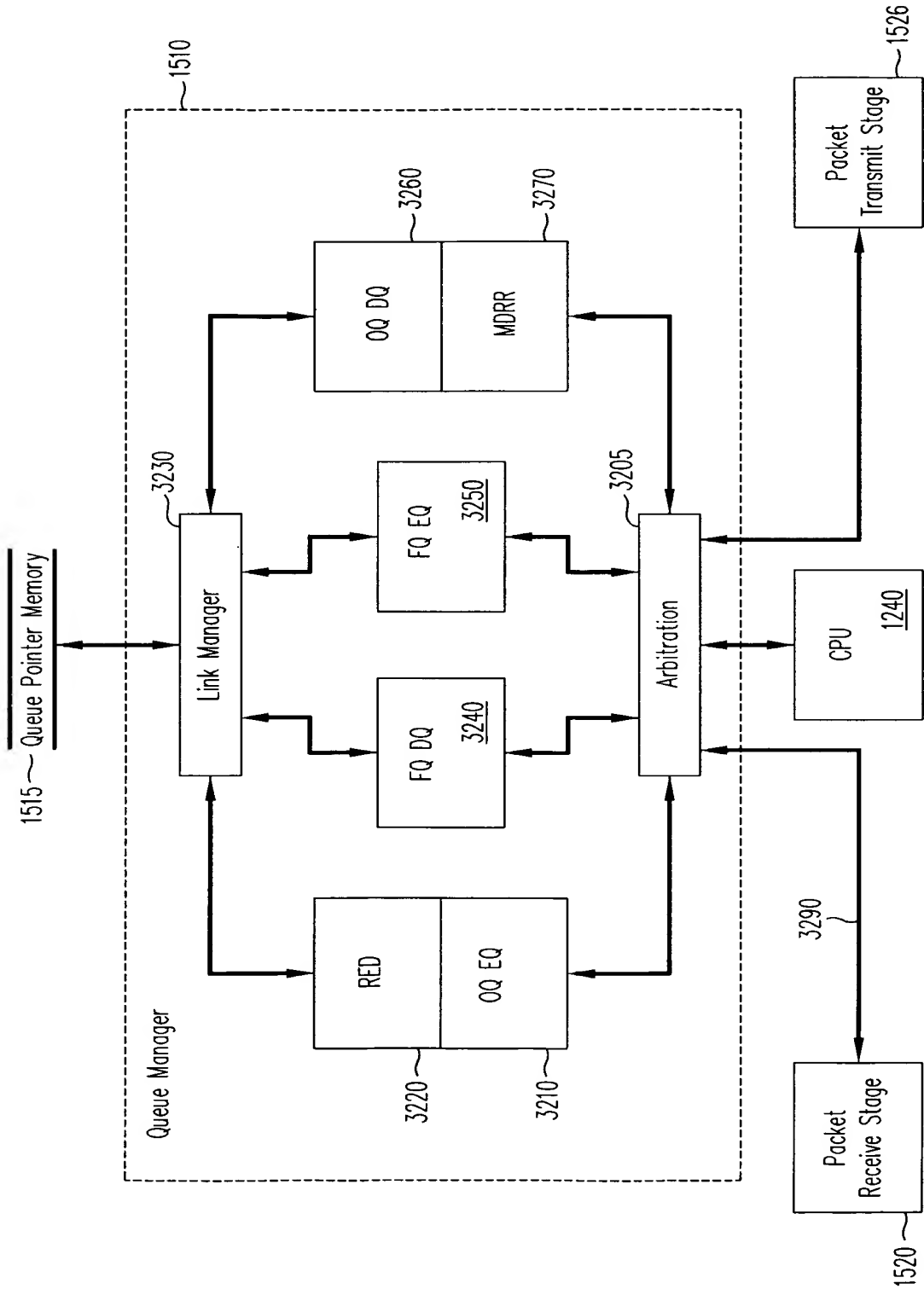


FIG. 32